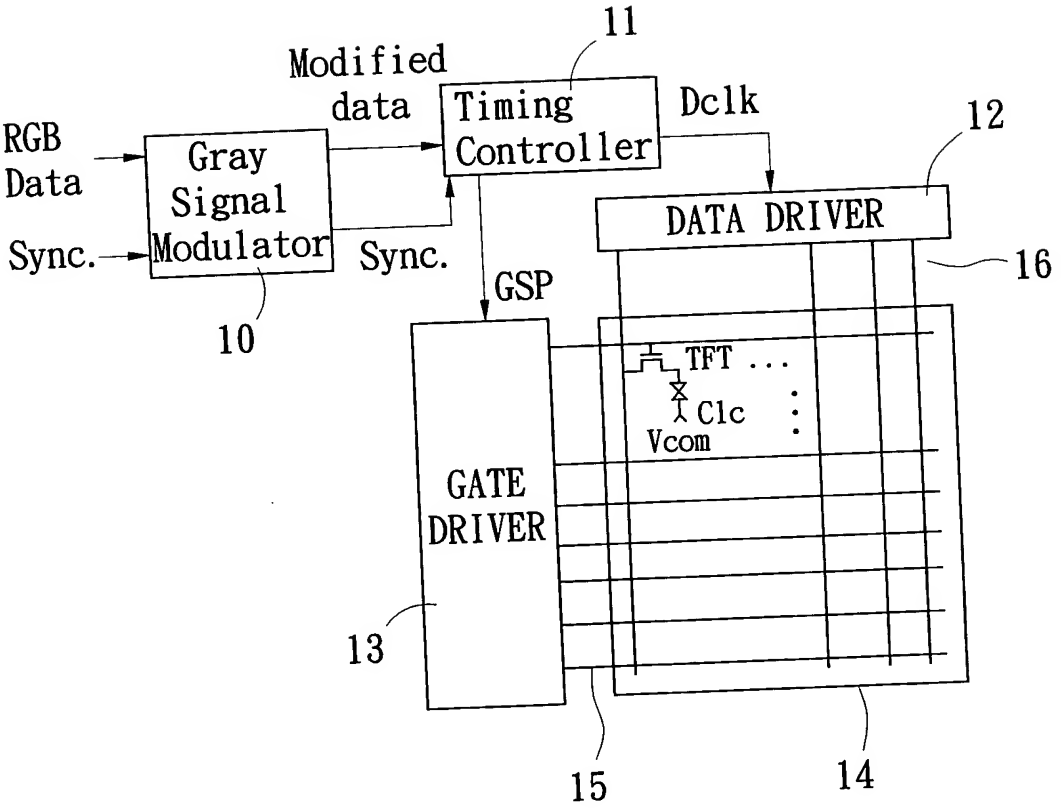

Fig. 1 (Prior Art)

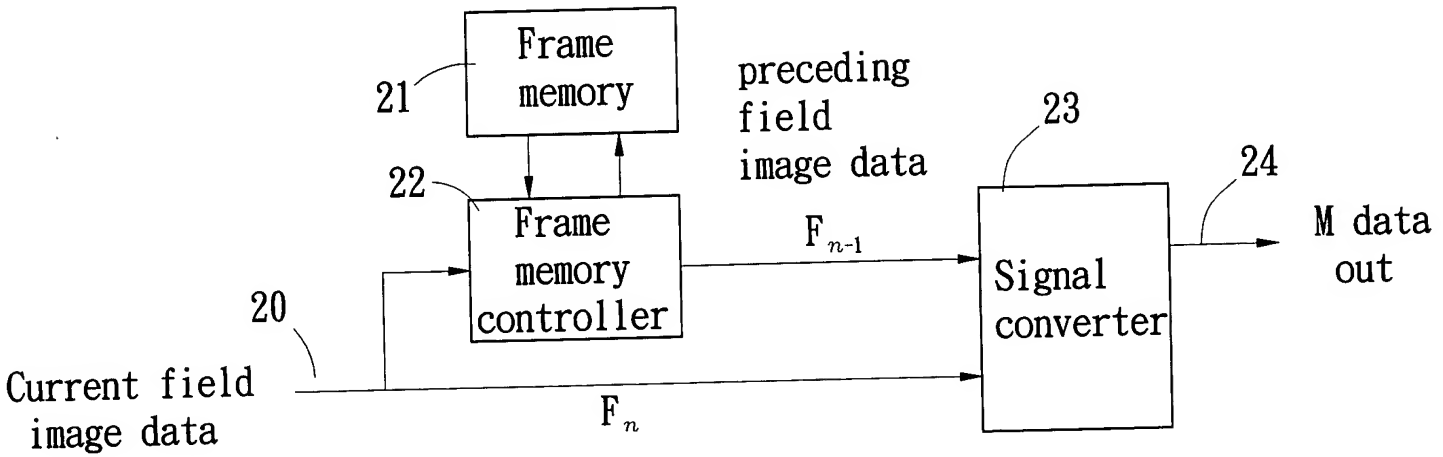

Fig. 2 (Prior Art)

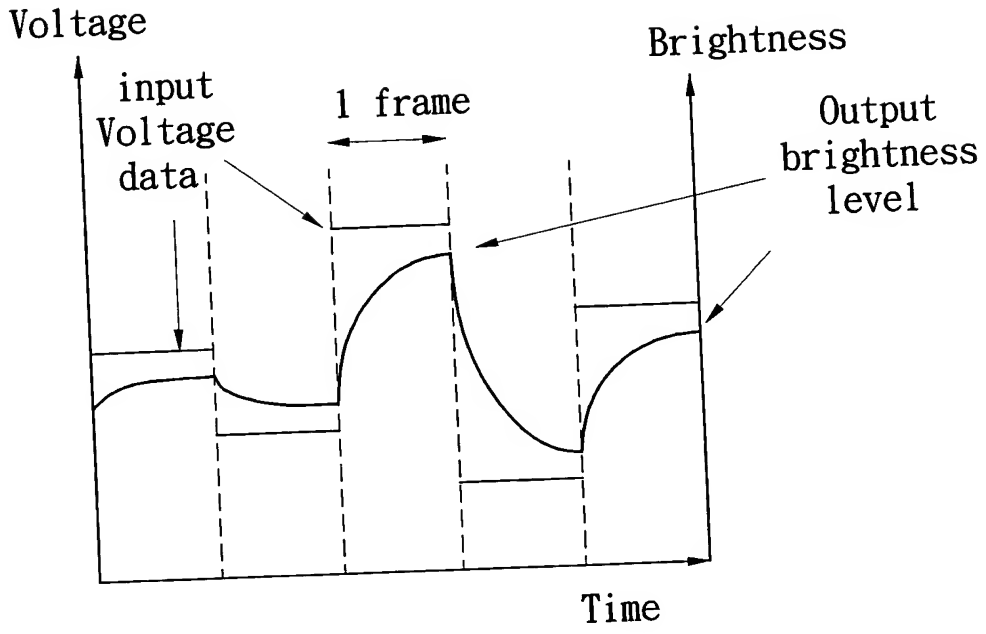

Fig. 3A (Prior Art)

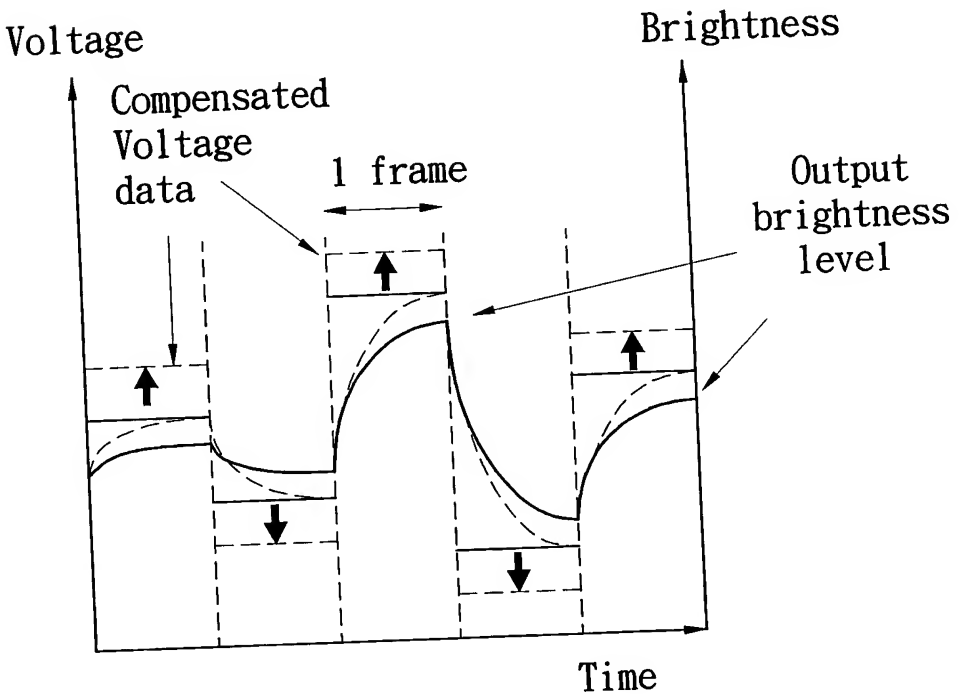

Fig. 3B (Prior Art)

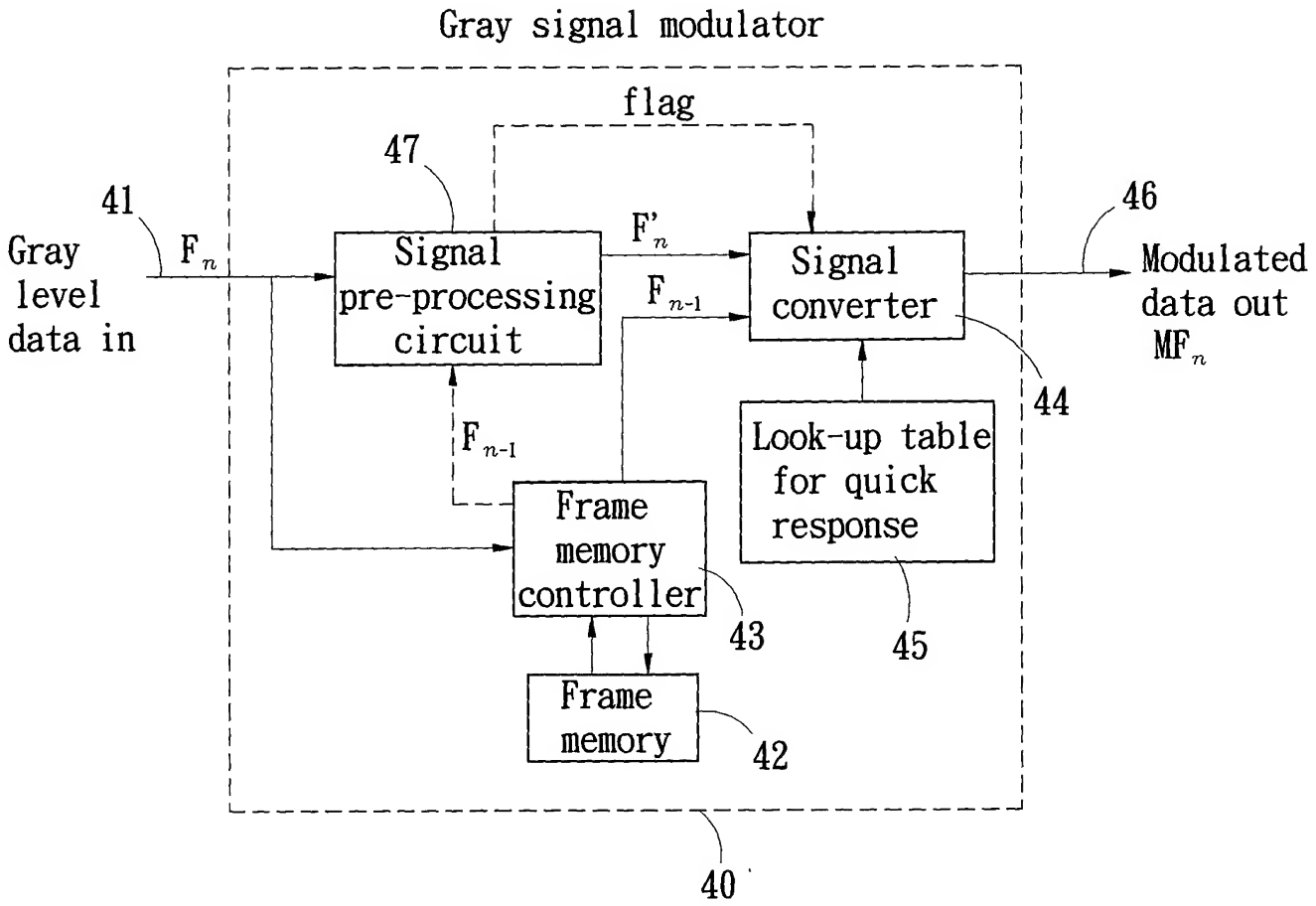
Gray signal modulator
flag
47
41
Gray level data in
F_n
Signal pre-processing circuit
F'_n
F_{n-1}
Signal converter
46
Modulated data out MF_n
44
F_{n-1}
Look-up table for quick response
Frame memory controller
43
45
Frame memory
42
40

Fig. 4

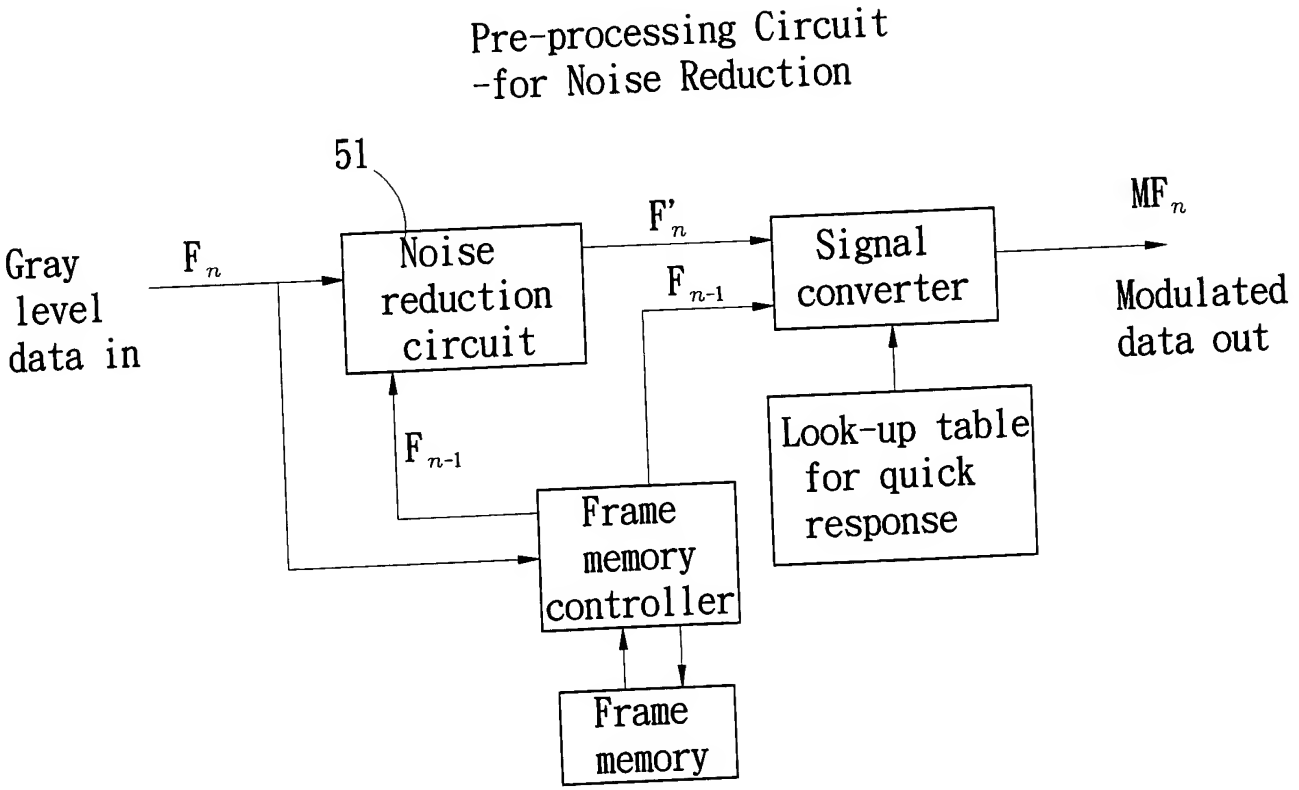
Pre-processing Circuit
-for Noise Reduction
51
Gray
level
data in
F_n
Noise
reduction
circuit
F'_n
F_{n-1}
Signal
converter
MF_n
Modulated
data out
F_{n-1}
Look-up table
for quick
response
Frame
memory
controller
Frame
memory

Fig. 5

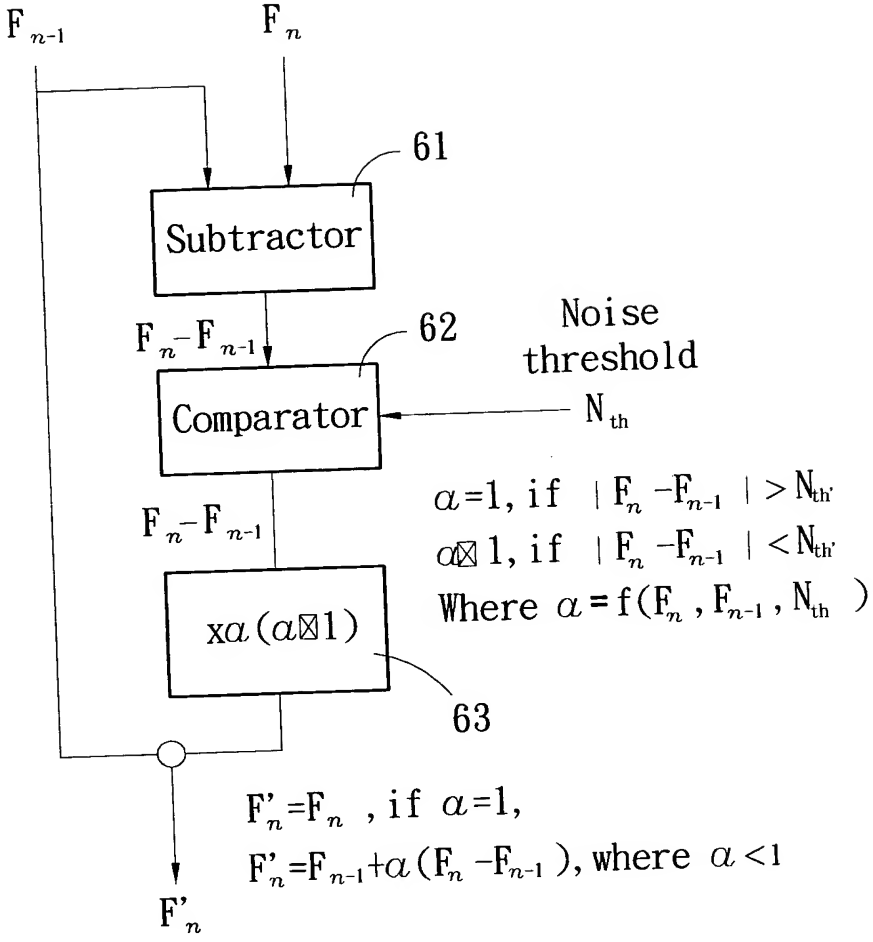
F_{n-1}
F_n
61
Subtractor
$F_n - F_{n-1}$
62
Noise threshold
Comparator
N_{th}
$\alpha=1$, if $|F_n - F_{n-1}| > N_{th}$
$\alpha \boxtimes 1$, if $|F_n - F_{n-1}| < N_{th}$
Where $\alpha = f(F_n, F_{n-1}, N_{th})$
$F_n - F_{n-1}$
$x\alpha$ ($\alpha \boxtimes 1$)
63
$F'_n = F_n$, if $\alpha=1$,
$F'_n = F_{n-1} + \alpha(F_n - F_{n-1})$, where $\alpha < 1$
F'_n

Fig. 6A

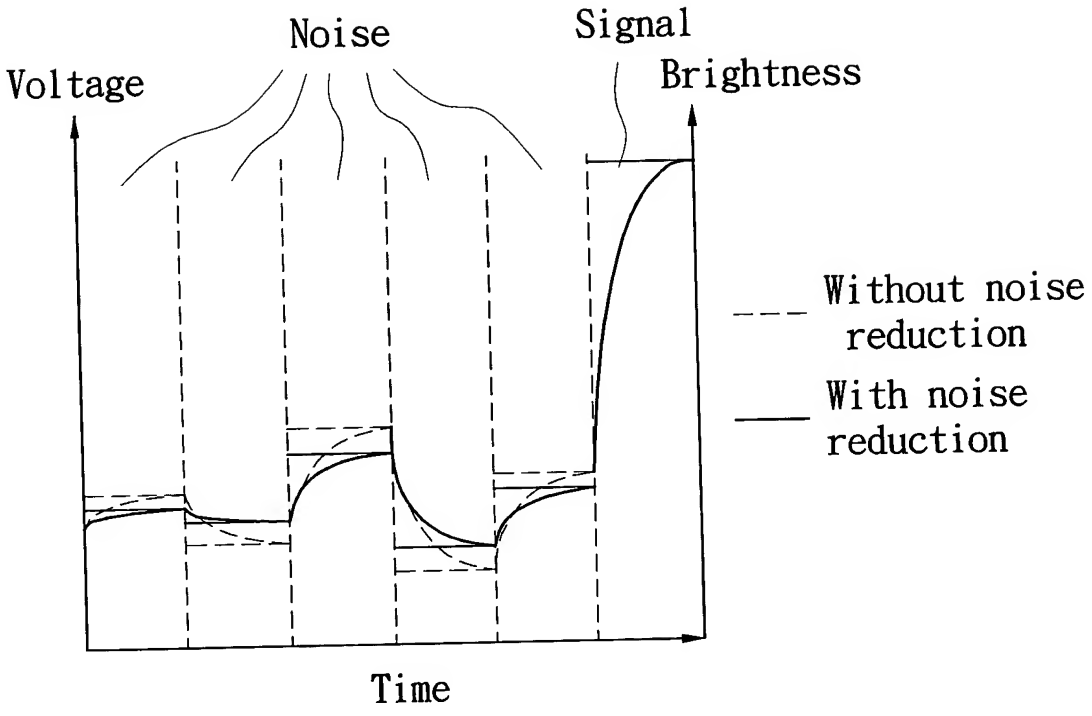
Noise
Signal
Voltage
Brightness
Without noise reduction
With noise reduction
Time

Fig. 6B

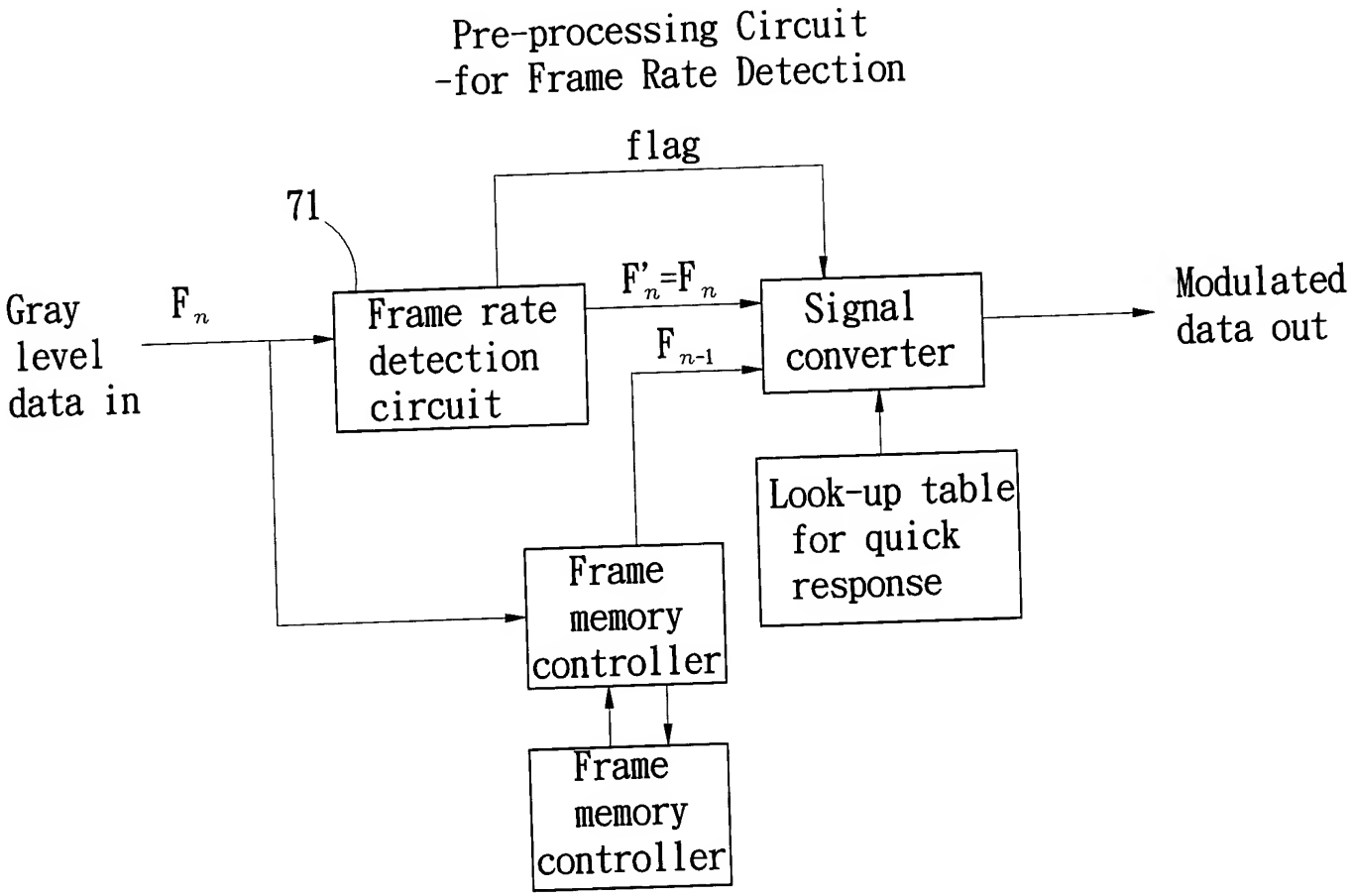
Pre-processing Circuit
-for Frame Rate Detection
flag
71
Gray
level
data in
F_n
Frame rate
detection
circuit
$F'_n=F_n$
F_{n-1}
Signal
converter
Modulated
data out
Look-up table
for quick
response
Frame
memory
controller
Frame
memory
controller

Fig. 7

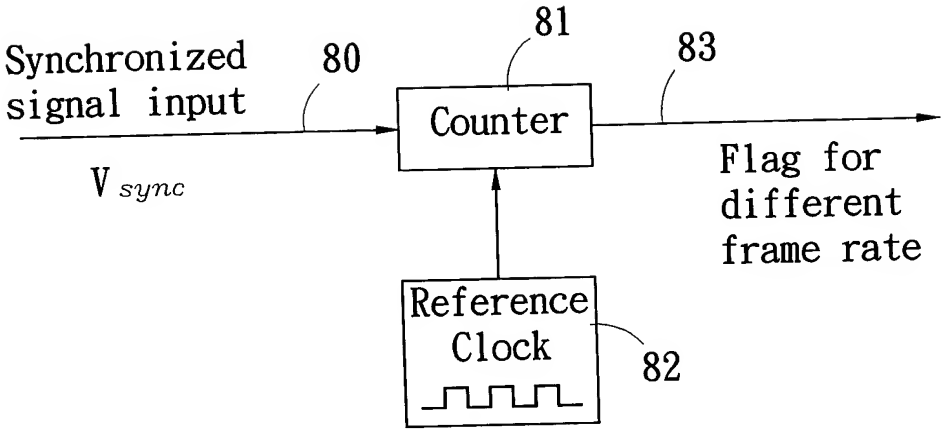
Synchronized
signal input
80
81
Counter
83
Flag for
different
frame rate
V sync
Reference
Clock
82

Fig. 8